

Application No. 10/788815

June 1, 2006

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CLMPTO

1. (Currently Amended) A Semiconductor device comprising:

- a semiconductor substrate,
- an insulating layer on top of said substrate,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulating layer,
- a drain runner arranged on top of the insulator layer above said drain region,
- a source runner arranged on top of the insulator layer above said source region,
- a gate runner arranged on top of the insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region, and
- a second coupling structure comprising a via for coupling said source runner with said source region and a barrier metal layers layer arranged at the bottom of said via and within said insulating layer, wherein the barrier metal layer comprises a first horizontal bottom layer adjacent said via and a side wall being rectangular to and surrounding said first horizontal bottom layer and said side wall is spaced apart from said via.

2. (Previously Presented) The Semiconductor device as claimed in Claim 1, wherein said first coupling structure further comprises barrier metal layers arranged at the bottom of said via.

3. (Original) The Semiconductor device as claimed in Claim 1, wherein said first and second coupling structure further comprise barrier metal layers arranged at the top of said via.

4. (Original) The Semiconductor device as claimed in Claim 2, wherein said bottom barrier metal layer has a cross-sectional profile of a saucer around said via.

5. (Original) The Semiconductor device as claimed in Claim 4, wherein the bottom barrier metal layer comprises side walls that enclose said via.

6. (Canceled)

7. (Original) The Semiconductor device as claimed in Claim 2, wherein the bottom barrier metal layer consists of Titanium-Titanium nitride.

8. (Original) The Semiconductor device as claimed in Claim 3, wherein the top barrier metal layer consists of Titanium-Platinum.

9. (Original) The Semiconductor device as claimed in Claim 1, wherein the via comprises tungsten.

10. (Original) The Semiconductor device as claimed in Claim 1, further comprising a sinker structure that reaches from the top to the bottom of said substrate.

11. (Original) The Semiconductor device as claimed in Claim 10, further comprising a backside metal layer arranged on the bottom surface of said substrate.

12. (Original) The Semiconductor device as claimed in Claim 1, further comprising a well structure surrounding said source region.

13. (Withdrawn) The Semiconductor device as claimed in Claim 1, further comprising a substrate via within said source area located under said source runner reaching from the top of said substrate to the bottom of said substrate.

14. (Withdrawn) The Semiconductor device as claimed in Claim 13, wherein said substrate via is filled with Tungsten or copper.

15. (Withdrawn) The Semiconductor device as claimed in Claim 14, further comprising a backside metal layer arranged on the bottom surface of said substrate and a barrier metal layer between said Tungsten or copper filled substrate via and said backside metal layer.
16. (Withdrawn) The Semiconductor device as claimed in Claim 14, further comprising a well structure surrounding said source region.
17. (Withdrawn) The Semiconductor device as claimed in Claim 2, wherein said barrier metal layer between the source region and the via is extended to form a field plate in such a way that it covers at least partly said gate.
18. (Withdrawn) The Semiconductor device as claimed in Claim 17, wherein the field plate covers part of the top surface of the gate and the side of the gate facing the drain runner.
19. (Withdrawn) The Semiconductor device as claimed in Claim 18, wherein the field plate is coupled with the barrier metal layer at a single location.
20. (Withdrawn) The Semiconductor device as claimed in Claim 17, wherein the field plate extends from the barrier metal layer to cover part of the left, top and right side of the gate.
21. (Withdrawn) The Semiconductor device as claimed in Claim 1, wherein the first coupling structure comprises a plurality of vias.
22. (Withdrawn) The Semiconductor device as claimed in Claim 1, wherein the second coupling structure comprises a plurality of vias.
23. (Withdrawn) The Semiconductor device as claimed in Claim 17, wherein the field plate comprises at least one cut out area.
24. (Original) The Semiconductor device as claimed in Claim 1, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

CLAIMS 25-35 (CANCELLED)

36. (Currently Amended) A Semiconductor device comprising:

- a semiconductor substrate,
- an insulator layer on top of said substrate,
- a lateral field effect transistor comprising a drain region and a source region arranged in said substrate and a gate arranged above said substrate within said insulator layer,
- a drain runner arranged in said insulator layer above said drain region,
- a source runner arranged in said insulator layer above said source region,
- a gate runner arranged in said insulator layer outside an area defined by said drain runner and said source runner,
- a first coupling structure comprising a via for coupling said drain runner with said drain region,
- a second coupling structure comprising a via for coupling said source runner with said source region and a barrier metal layers arranged at the bottom of said via and within said insulating layer, wherein the barrier metal layer comprises a first horizontal bottom layer adjacent said via and a side wall being rectangular to and surrounding said first horizontal bottom layer and said side wall is spaced apart from said via,
- wherein said first and second coupling structure further comprise barrier metal layers arranged at the top and the bottom of said via,
- a sinker structure that reaches from the top to the bottom of said substrate, and
- a backside metal layer arranged on the bottom surface of said substrate.

37. (Withdrawn) The Semiconductor device as claimed in Claim 36, wherein said barrier metal layer between the source region and the via is extended to form a field plate in such a way that it covers at least partly said gate.

38. (Original) The Semiconductor device as claimed in Claim 36, wherein the substrate comprises a p+ substrate and p- epitaxial layer.

CLAIMS 39-95 (CANCELLED)